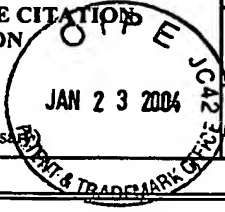


PTO-1449 REPRODUCED		ATTORNEY DOCKET NO. 2037.2038-001		APPLICATION NO. 10/647,664	
INFORMATION DISCLOSURE CITATIONS IN AN APPLICATION January 9, 2004 (Use several sheets if necessary)		FIRST NAMED INVENTOR Tony Mai		FILING DATE August 25, 2003	
		EXAMINER		CONFIRMATION NO. 2135	
				GROUP 2631	



U.S. PATENT DOCUMENTS				
EXAM- INER INI- TIAL	REF. NO.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
EB	AA	6,314,052 B2	11/06/01	Foss <i>et al.</i>
EB	AB	6,314,150 B1	11/06/01	Vowe
EB	AC	6,330,296 B1	12/11/01	Atallah <i>et al.</i>
EB	AD	6,337,590 B1	01/08/02	Miller
EB	AE	6,448,820 B1	09/10/02	Wang <i>et al.</i>
EB	AF	6,549,041 B2	04/15/03	Waldrop
	AG			
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	AC3			

EXAMINER /Emmanuel Bayard/ (10/04/2006)	DATE CONSIDERED
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EB	AR	C.H. Kim <i>et al.</i> "A 64 Mbit, 640 Mbyte/s bidirectional Data Strobed, Double-Data-Rate SDRAM with a 40-mW DLL for a 256-Mbyte System", <i>IEEE J. Solid State Circuits</i> , 33(11), November 1998.
EB	AS	Hsiang-Hui Chang <i>et al.</i> "A Wide Range Delay-Locked Loop With a Fixed Latency of One Clock Cycle", <i>IEEE J. Solid State Circuits</i> , 37(8), August 2002.
EB	AT	Hongil Yoon <i>et al.</i> "A 2.5V, 333-Mb/s/pin, 1-Gbit, Double-Data-Rate Synchronous DRAM", <i>IEEE J. Solid State Circuits</i> , 34(11), November 1999.
EB	AU	Se Jun Kim, <i>et al.</i> "A low-Jitter Wide-Range Skew-Calibrated Dual-Loop DLL Using Antifuse Circuitry for High-Speed DRAM", <i>IEEE J. Solid State Circuits</i> , 37(6), June 2002.
	AV	
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EXAMINER /Emmanuel Bayard/ (10/04/2006)	DATE CONSIDERED
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